PerfectVIPs
Right Tools... Perfect Chip

Single Root IO Virtualization VIP

DATASHEET
Rev. 1.0

GENIE-SR-IOV

SR-IOV VERIFICATION IP

OVERVIEW

SR-IOV provides a mechanism by which a Single Root Function (for example a single Ethernet Port) can appear to be multiple separate physical devices. A SR-IOV-capable device can be configured (usually by the VMM/PCIM) to appear in the PCI configuration space as multiple functions, each with its own configuration space complete with Base Address Registers (BARs). The VMM assigns one or more VFs to a VM by mapping the actual configuration space the VFs to the configuration space presented to the virtual machine by the VMM/PCIM.

The Genie-SR-IOV Verification IP Products is the industry's most comprehensive verification solution for SR-IOV based designs. Its intelligent **Verification Engine**, integrated **Interface Inspector** and comprehensive **Compliance Suite** provide the perfect combination of tools to ensure first silicon success.

The **Genie-SR-IOV VIP** provides a quick and efficient way to verify any SR-IOV based PCIe design. It supports SR-IOV revision 1.1 specifications and tests all layers of SR_IOV and PCIe protocol – Phy, Link, Transport and Application. Genie-SR-IOV provides a complete verification solution that includes system verilog based bfm & UVM methodology.

The Genie-SR-IOV VIP provides:

- Bus Functional Models
- Directed and Random Transaction Generator
- Frame & Primitive Generator
- Error Injector
- Callbacks
- Monitor/Checker
- Report Generator

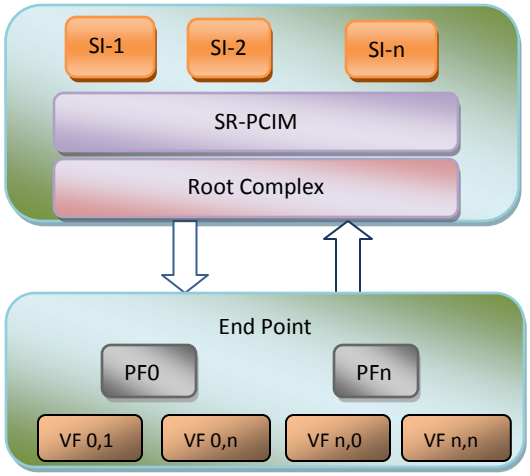

Fig 1: SR-IOV Verification Environment

FEATURES

❖ provide configurable numbers of independent VFs, each with its own PCI Configuration space	❖ Supports MSI, MSI-X, Address Range Isolation
❖ SR-IOV 1.1 compliant	❖ Supports baseline error reporting
❖ Supports FLR	❖ Supports re-Initialization & reallocation
❖ Does VF, BAR, supported page size discovery & configuration	❖ Supports Functional Dependencies
❖ Supports AT & ATPT	❖ System level and block level testing
❖ Scoreboard capability for data integrity checking	❖ Functional coverage & coverage report
❖ Ability to enable or disable specific error checks and violations	❖ Configurable test generation for constrained random, directed and error testing
❖ Programmable parameters through configurable Knobs	❖ Ability to control and change packet value during transmission through each layer
❖ User configurable reports for logging events and transactions	❖ Can be configured as SR-IOV capable Device or SR-IOV capable Root complex
❖ Automatic and user configurable Callback capability	❖ Packet corruption at bit level granularity
❖ Comprehensive Compliance Suite	❖ Supports UVM Methodology

PRODUCT DETAILS

SR-IOV capable End Point Features

- BFM can be configured as EndPoint.
- Supports 8 functions with configurable number of virtual functions (VFs) from testcase.
- Implements PF's extended configuration space supporting SR-IOV capability and individual configuration space for all VFs
- Implements all internal routing between PFs and VFs.

SR-IOV capable Root Complex Features

- BFM can be configurable as RC
- Multiple System images can be created above RC
- Implements PCIM
- APIs to inject user-defined packets into different layers for transmission
- Randomized or Directed error injection

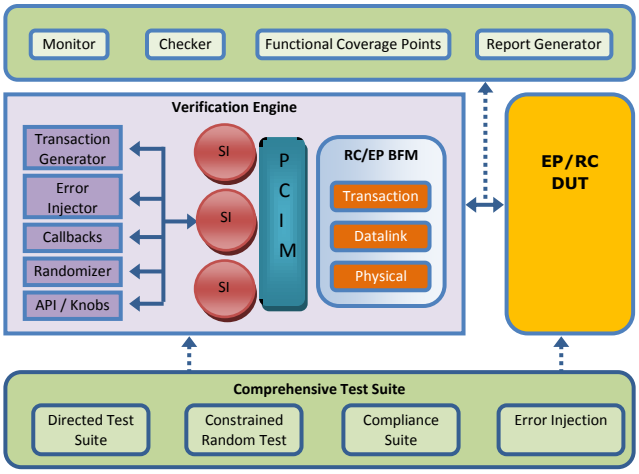

Fig. 3: SR-IOV Verification Environment

SR-IOV capable Monitor

- SR-IOV monitor tracks and observes all traffic on the bus. It generates LOG files that are user configurable to customize information reported. It has the capability to program file names for logging information. It also supports Performance Analysis and Functional Coverage.

SR-IOV capable Checker

- SR-IOV checker provides bus-level protocol checking capability. It performs real-time reporting of errors on the clock in which the End symbol of a packet is received.

SR-IOV capable SB (Scoreboard)

- SR-IOV scoreboard holds predicted data and DUT data, Compares both for data integrity check

SR-IOV COMPLIANCE SUITE	SR-IOV SOLUTIONS
Developed by PerfectVIPs to thoroughly exercise SAS designs, the compliance suite is a comprehensive verification test suite that provides hundreds of test cases. ▪ Verifies all VFs, their interdependencies, performs all PCIe related transactions on each VFs ▪ Provides comprehensive coverage targeted at VFs, with all kinds of interrupts, transactions and error scenarios ▪ Identifies all protocol violations(PCIe) ▪ Provides directed and constrained random regression testing capability	The following SR-IOV solutions are available. Verification IP: ▪ SR-IOV EP VIP ▪ SR-IOV Host set(RC, PCIM, SI) VIP ▪ Interface Inspector ▪ Checker/coverage/scoreboard Compliance Suites: ▪ RC Test Suite ▪ EP Test Suite

SUPPORTED SIMULATORS: ALDEC CADENCE MENTOR SYNOPSYS

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